CLAIMS

What is claimed is:

1. A multi-chips module package, comprising:

a main substrate having an upper surface and a plurality of contacts;

a first chip disposed above the main substrate, the first chip having a first active surface, a first back surface opposite to the first active surface, a first wire-bonding pad and a first bump-bonding pad, wherein the first wire-bonding pad and the first bump-bonding pad are formed on the first active surface;

a second chip disposed above the main substrate, the second chip having a second active surface, a second back surface opposite to the second active surface, a second wire-bonding pad and a second bump-bonding pad, wherein the second wire-bonding pad and the second bump-bonding pad are formed on the second active surface;

an interconnection substrate having a first chip-connecting contact, a second chip-connecting contact and a circuit connecting the first chip-connecting contact and the second chip-connecting contact;

a first bump, the first bump interposed between the first chip-connecting contact and the first bump-bonding pad;

a second bump, the second bump interposed between the second chip-connecting contact and the second bump-bonding pad; and

a plurality of wires, the wires electrically connecting the first wire-bonding pad and the second wire-bonding pad to the contacts respectively.

2. The multi-chips module package of claim 1, further comprising an encapsulation

covering the first chip, the second chip, and the upper surface of the main substrate.

3. The multi-chips module package of claim 1, wherein the interconnection substrate is a die-substrate.

4. The multi-chips module package of claim 1, wherein the main substrate is a lead-frame.

5. The multi-chips module package of claim 1, wherein the main substrate is a quad flat non-leaded lead-frame.

6. The multi-chips module package of claim 1, wherein the first bump is a metal bump.

7. The multi-chips module package of claim 1, wherein the second bump is an electrically conductive plastic bump.

8. The multi-chips module package of claim 1, wherein the material of the second bump comprises epoxy.

9. The multi-chips module package of claim 1, wherein the interconnection substrate is an organic substrate.

10. The multi-chips module package of claim 6, wherein the metal bump is a gold bump.

11. The multi-chips module package of claim 6, wherein the metal bump is a lead-free bump.

12. The multi-chips module package of claim 1, wherein the main substrate further comprises two chip pads for carrying the first chip and the second chip.

13. The multi-chips module package of claim 1, further comprising a plurality of

solder balls attached to ball pads of the lower surface of the main substrate.

14. The multi-chips module package of claim 1, further comprising a passive component disposed on the interconnection substrate.

15. The multi-chips module package of claim 14, wherein the passive component is a capacitor.

16. The multi-chips module package of claim 1, further comprising a passive component embedded in the interconnection substrate.

17. The multi-chips module package of claim 2, wherein the interconnection substrate is exposed out of the encapsulation.

18. A multi-chips module package, comprising:

a main substrate having an upper surface and a plurality of contacts;

a first chip disposed above the main substrate, the first chip having a first active surface, a first back surface opposite to the first active surface, a first wire-bonding pad and a first bump-bonding pad, wherein the first wire-bonding pad and the first bump-bonding pad are formed on the first active surface;

a second chip disposed above the main substrate, the second chip having a second active surface, a second back surface opposite to the second active surface, a second wire-bonding pad and a second bump-bonding pad, wherein the second wire-bonding pad and the second bump-bonding pad are formed on the second active surface;

an interconnection substrate having a first chip-connecting contact, a second chip-connecting pad and a circuit connecting the first chip-connecting contact and the second chip-connecting contact, the interconnection substrate attached to the first chip and the second chip directly through solder materials; and

a plurality of wires, the wires connecting the first wire-bonding pad and the second wire-bonding pad to the contacts respectively.

19. The multi-chips module package of claim 18, further comprising an encapsulation covering the first chip, the second chip, and the upper surface of the main substrate.

20. The multi-chips module package of claim 18, wherein the interconnection substrate is a die-substrate.

21. The multi-chips module package of claim 20, wherein the interconnection substrate is exposed out of the encapsulation.